A 12-BIT PSEUDO-DIFFERENTIAL CURRENT-SOURCE RESISTOR-STRING HYBRID DIGITAL-TO-ANALOGUE CONVERTER WITH LOW PASS RC FILTER

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LIST OF ABBREVIATIONS

DAC	Digital-to-Analogue Converter
DNL	Differential Non-Linearity
INL	Integral Non-Linearity
MSB	Most Significant Bit
LSB	Least Significant Bit
SRD	Swing Reduced Drivers
CFT	Clock Feed-Through
PTM	Predictive Technology Model
W/L	Width-to-Length Ratio
V_{SG}	Source-Gate Voltage
VDD	Supply Voltage
GND	Ground
C_{GD}	Gate-Drain Overlap Capacitance
SNR	Signal-to-Noise Ratio
SSN	Simultaneous Switching Noise
di/dt	Instantaneous Rate of Current Change
F_c	Cutoff frequency
F_g	Glitch frequency

A 12-BIT PSEUDO-DIFFERENTIAL CURRENT-SOURCE RESISTOR-STRING HYBRID DIGITAL-TO-ANALOGUE CONVERTER WITH LOW PASS RC FILTER

ABSTRACT

Major concern in a high speed digital to analogue converter (DAC) is the occurrence of glitches which limiting the performance of the converter. As technology moving toward higher speed and smaller sizes, eliminating glitches is very important to ensure maximum performance of a DAC. Glitches limit maximum performance of a DAC especially in term of switching speed where it restrict the high speed performance of DAC. In some cases glitches can cause the converter to be unusable. This work discusses the design methodology to further improve glitches in the existing hybrid DAC with current-limited swing reduced driver circuit. The 12 bit hybrid DAC architectures is composed of 8-LSB binary-weighted resistor and 4-MSB thermometer coding in order to have optimize performance. The improved DAC design is accomplished by incorporating a Low Pass RC filter which function to attenuate the amplitude of the glitch that exceed the cutoff frequency, F_c . Simulation results shows that glitch impulse area was 9.1046pVs while peak glitch is only 1.08mV. This results indicates that this design achieves 70% improvement in glitch impulse area reduction compared with original version DAC and showing improvement of 47.71% compared to DAC with only current limited SRD. Overall, this project have successfully achieves lower glitch impulse area.

12-BIT PSEUDO-PENGAMIRAN SUMBER-ARUS RENTETAN PERINTANG HIBRID PENUKAR DIGIT-KE-ANALOG BESERTAKAN PENAPIS LALUAN RENDAH

ABSTRAK

Isu utama yang menghadkan prestasi penukar digital ke analog (DAC) adalah kewujudan glic. Di kala teknologi sekarang bergerak ke arah saiz yang lebih kecil, kelajuan yang lebih pantas, ia adalah sangat penting untuk memastikan isu glic di minimalkan. Kerja ini membincangkan cara-cara yang terbaik untuk mengurangkan kewujudan glic di dalam sistem 12-bit pseudo-pengamiran sumber-arus rentetan-perintang hibrid DAC. Glic menghadkan prestasi DAC terutamanya berkenaan dengan kelajuan penukaran digital ke analog. 12-bit DAC yang dinyatakan terdiri daripada kombinasi skim perintang binari berwajaran dan termometer pengekodan terbahagi kepada 8-LSB dan 4-MSB segmen. Untuk projek ini, glic berjaya di kurangkan dengan menambah penapis laluan rendah di bahagian hujung DAC. Kesimpulannya, penapis elekrik laluan rendah ini boleh di manipulasi untuk menapis signal tinggi yang tidak diingani dan hanya membenarkan signal rendah untuk lalu ke DAC. Berdasarkan simulasi didapati tenaga glic adalah 9.1046pVs dan glic amplitud 1.08m V. Ini membuktikan bahawa reka bentuk DAC yang disertakan dengan penapis laluan rendah ini berjaya mengurangkan glic sebanyak 70% dibandingkan dengan reka bentuk DAC asal dan 47.71% pembaikan dibandingkan dengan reka bentuk DAC dengan arus terhad pemandu.

CHAPTER 1

INTRODUCTION

1.1 Overview

A Digital to Analogue Converter (DACs) is a device responsible to convert digital information which comprised of series of 1 and 0 into an analogue signal. Nowadays, most technology required DAC to function such as headphones, television, mobile phones and etc. DAC application is influenced by three parameter; resolution, maximum sampling frequency and accuracy. As digital processing technology becomes more important and widely used, the DAC are built with lower power consumption, high resolution data and high speed operation. Unfortunately, the DAC performance is affected by few limiting factor such as Integral Non Linearity (INL) error, Differential Non Linearity (DNL) and glitches energy [1]. To be more specific DACs are sensitive to vibrant effects such as glitches. In fact, glitches can limit overall spectral operation of the DAC making it unusable for specific applications [1].

There are many DAC architectures each have their own pros and cons during performing operation. Therefore, in order to have best design with most advantages and least disadvantages a 12 bit hybrid DAC composed of binary weighted resistor DAC, thermometer coding DAC and current steering DAC is presented [1]. This hybrid DAC was proven by [2] to have better performance in monotonicity, linearity (DNL and INL) and glitch impulse area.

As DAC architectures evolved toward high speed, low power and voltage consumption, the influence of glitch becomes more important. It is known that glitch impulses occur at major carry transition. A major carry transition is defined as a single code transition causing most significant bit (MSB) to change due to transitioning of the lower bits [1]. As a solution to reduce glitch impulse area a low pass RC filter are implemented in the DAC design. The low pass RC filter will attenuate the amplitude of the glitches. It will only allow low frequencies signal to pass through and will filter out all the high frequency. In this case, it will allow frequencies only from baseband to the cut off frequencies of about 2.18MHz and attenuates other higher signals. With removal of high frequency the energy of glitch reduces. Therefore, a glitch improvement in DAC achieved by incorporating hybrid DAC and SRD with a low pass RC filter.

1.2 Problem Statement

1.2.1 Problem Identification

Major drawback with DAC is the occurrence of glitches that are impacting the overall performance of a high speed DAC. As technology are moving to high speed and low power consumption, the impact of glitch become very significant. In most cases, DAC operation is affected by non-idealities which limit the performance and the system including it.

Existence of glitch in high speed DAC can deteriorate the overall performance of the converter making it unusable for certain application [2]. It can very much impact the conversion speed of the DAC as glitches limit the DAC switching speed therefore restricting the high speed performance of the DAC [3]. Glitch too have the potential to cause non monotonic behavior due to timing errors and device mismatches [3]. As mentioned in [1] glitch are highest during major code transition, change in input code will cause the output code to be glitch dependent. Therefore it is crucial to remove as much glitches as possible from the converter.

1.2.2 Project Significance

This project is implementing a deglitching method into the DAC to ensure it have the maximum performance in term of high speed and resolution at a lower power consumption. A low pass RC filter is added to the DAC to filter out all the unwanted signal or frequency. The Hybrid DAC with Low Pass RC filter is represented using Predictive Technology Model (PTM) 45nm 1.1v CMOS process technology.

1.3 Objectives

The main objectives of this project is to design a deglitching circuit to further improve the existing glitch of the aforementioned 12 bit hybrid DAC with current limited SRD. The aims is to ensure the DAC fulfilled following criteria:

1. To design a Hybrid DAC that have lower peak glitch and glitch impulse area by adding a Low Pass RC filter. This project is targeting an improvement of more than 70% meaning both peak glitch and net glitch impulse area should be lower than 5mV and 10pVs as compared to the Original DAC.
2. To design a Hybrid DAC with Low Pass RC Filter that have a layout size within range of 250µmx250µm to 300µmx300µm.

1.4 Project Scope

This project is basically aiming to ensure maximum performance of the DAC by reducing glitches to ensure low power consumption, higher speed and resolution. To reduce glitches, a low pass RC filter is incorporated in the hybrid DAC design to further improve the performance. Do take note that this project will not be focusing on DNL and INL due to tools limitation. The simulation results is captured and compared with three existing design:

1. Original DAC Design
2. DAC with implementation of Swing Reduce Driver
3. DAC with implementation of Current-limited Swing Reduced Driver

The aforementioned 12 bit hybrid DAC architecture is implemented on Linear Technology spice IV by using PTM 45nm 1.1V CMOS process technology. To simplify study and ease of troubleshooting, the overall circuit design is divided into few different

block such as DAC reference block, DAC decoder block, Single DAC block and DAC multiplexer block. Simulation on the original version of DAC is performed and results is captured. The glitches energy and peak glitch will be the main focus for this project.

Secondly, current switches with swing reduced drivers (SRDs) was incorporated into the DAC to reduce the glitches [4]. Similar process technology of PTM 45nm 1.1V CMOS is implemented. Simulation is performed and results is obtain. The glitches peak values and glitches energy is also measured for further comparison and discussion.

Thirdly, designs is incorporated with a new version of SRD called current limited SRD [1]. This design was an improvement of the previous swing reduced driver (SRDs). Simulation is performed with PTM 45nm 1.1V CMOS process technology. The outcome of this design is proven to have better performance in low glitch and low power consumption. The results obtained is compared with results of the previous SRD design.

The architectures of the previous methodologies on glitch improvement and operation of each circuit is studied and understand thoroughly. With the advantages and disadvantages from each previous topology and as the sources of glitches is known, a new method of deglitching called Low Pass RC filter is implemented into the above-mentioned DAC hybrid circuit. Simulation is performed on the hybrid DAC with current limited SRD and the Low Pass RC filter. Simulation is done with PTM 45nm 1.1V CMOS process technology. The obtained results are compared with the three previous topology mentioned.Lastly, comparison and discussion of results obtained from the Original DAC

version, Hybrid DAC with SRD, Hybrid DAC with current limited SRD and the new design of hybrid DAC with current limited SRD and low pass RC filter. The glitches energy from each of the design will be the main focus of discussion. The characteristics and benefits of the low pass RC filter is concluded and recommendation for further improvements is given

1.5 Thesis Outline

This project discusses, analyses and conclude the characteristic of glitches in a DAC and its architectures and provide a suitable method to improve the glitches. A Low Pass RC Filter circuit is incorporated in the hybrid DAC to reduce the glitches. The outcome of the improved design are compared with the previous design. This thesis is organized into 5 chapters beginning with the abstract, introduction that consists of problem statement, project objectives and scope of research, followed by the literature reviews, results and discussion. The summary for each chapters were discussed below:

Chapter 2 discusses the literature review where it presents overall specifications and concept of a DAC. The factor that influence the design of the DAC is also discusses here. This chapter also explain the 12 bit hybrid DAC architecture that comprises of three conventional DAC architectures; binary-weighted resistor DAC, thermometer coding DAC and current steering DAC. Besides, the overall circuit design of the 12 bit hybrid DAC are also discusses. The overall circuit is divided into few blocks; DAC references,

Single DAC, DAC decoder and DAC multiplexer. Function and characteristic of each block is explained. Other than that, the overview of glitch phenomenon and its characteristics are analyzed.

Chapter 3 focus on methodology that provides suitable method to reduce glitches in the 12 bits hybrid DAC. The Low Pass RC filter is designed and implemented in the 12-bits Hybrid DAC with current limited SRD. The architectures and circuit operation of the Low Pass RC filter are also being discussed in this chapter. Detail explanation and theory behind this filter and how it function to filter out the unwanted signals are also explained. This chapter also include the formula and equation used in designing the suitable RC filter.

Chapter 4 discusses results and discussion base on the simulation results obtained from previous DAC topology and the improved version DAC. The glitches from each DAC version are compared, meanwhile the glitches improvement of the 12-bits hybrid DAC with current-limited SRD and low pass RC filter are further discussed. This chapter will also discuss the advantages and disadvantages of each of the DAC design based on the glitch improvement achieved by each of the design.

Chapter 5 provides conclusion and future work where finding and data as presented in previous chapter especially on the improvement of glitches on the new DAC design with a Low Pass RC filter will be summarize. Comparison with previous DAC version also discussed. The future work to further enhance this project is also described.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

Digital-to-Analogue Converters (DACs) referred to a process where signals with few defined state (binary digital impulse of ones and zeros) are convert to an infinite number of state (analogue). DAC is used to decode digital signals into a meaningful analog output such as voice, music, or mechanical motion. There are many type of DAC architectures developed to perform conversion of digital signals to analogue signal in terms of current or voltage [1]. Each DAC architectures come with its own advantages and disadvantages. Thus, each DAC have different performance and limitations in term of linearity, monotonicity and glitch impulse area. This work will focus on glitch impulse area.

It is technically proven that a hybrid DAC will be able to give a better performance compared to a single DAC as stated in [5]. This is because hybrid DAC will achieve most of the advantages and least of the disadvantages from the conventional DAC architectures [5]. The 12 bit hybrid DAC for this thesis is consists of three conventional DACs, which are binary weighted resistor DAC, weighted current-steering DAC and thermometer coding DAC. Main disadvantages of single DAC is they tend to have a complex circuitry which causes latency and glitches occurrence [5].

The combination of these conventional DAC provides better linearity such as Differential Non Linearity (DNL) and Integral Non Linearity (INL) was achieved [5]. Besides hybrid DAC reduced occurrences of glitches and complexity of circuitry. Digital-to-Analogue Converters (DACs) are used to provide an interface between digital data sequence and the analogue signal. Many conventional DAC architectures had been developed to convert a digital data sequence in binary to an analogue signal in terms of current or voltage, this includes weighted current-steering DAC, binary-weighted resistor DAC and thermometer coding DAC. Each of the conventional DAC architecture has its pros and cons. Therefore, each of the conventional DAC has different limitations in static and dynamic performance, including linearity, monotonicity and glitch impulse area.

Glitch is an unwanted signals occurred at the output of the DAC. Glitches normally occurred as the DAC switches from one voltage to another. These glitches are minimal voltage spikes happened when DAC output a new voltage level. In traditional DACs architecture biggest glitch happens at the major transition i.e. 01 1111 1111 to 10 0000 0000 as discussed in [1]. This where most significant bit (MSB) convert from low to high and the rest of the bits changes from high to low, vice versa. Occurrence of glitches degrade performance of high speed DACs. A lot of design techniques have been proposed in hope to solve the glitch issues. This project will focus on implementing a Low Pass RC Filter which function to filter out the unwanted signal [6].

2.1.1 Predictive Technology Model

As today technology are shrinking in size (nanometer technology), a few factor that earlier had minimum impact on circuit performance are now necessary for improvement. Predictive technology model (PTM) allows primary device and circuit characterization by providing key insights into design research and advanced process in the upcoming technology [7]. PTM are suitable for high performance design in order to achieve a more accurate physical prediction by identifying the primary parameters and implementing important correlation between them [7]. PTM will cover other process choices and some earlier secondary effects that are crucial for future low power design. This include gate leakage current, multiple threshold technology, and temperature and body bias effects [8].

In this work, simulations were done by using nominal case model of PTM 45nm 1.1V CMOS process technology. This technology was chosen for the simplicity in usage and the ability to provide high accuracy in physical prediction. Beside the components provide in this technology is almost as accurate as the real devices.

2.2 Hybrid DAC Architecture

In this project, the hybrid DAC architecture will be based on at least two conventional DAC architectures. Each of the implemented DAC architectures will have its own advantages and disadvantages, thus hybrid DAC are developed to absorb most of

the advantages and least of the advantages. This 12-bit pseudo-differential current-source resistor-string hybrid DAC project implemented three type of DAC architectures; binary-weighted resistor DAC, thermometer coding DAC and weighted current steering DAC.

The binary-weighted resistor DAC be made up of series-connected resistors where values of resistor increased as the weighted digital input values increased. This method is chosen due to simplicity of the design and is suitable for a low resolution DAC with small digital input values [9]. However, this topology is not appropriate for high resolution application with large digital input values. High resolution DAC will required larger resistor values which is unreasonable due to overhead in overall area. Larger resistor will allow transistor mismatch to occur thus will give impact on linearity performance of the DAC. Meanwhile, the current steering DAC consists of a number of current sources connected in parallel. In this method, each current sources connected to a switch that controlled by the digital input. Besides, current steering DAC do not required a decoder which simplifies the circuit and explained the higher speed. Nevertheless, the current steering DAC has its limitations too such as glitch energies and occurrence of current mismatch as results of process variation [10].

The thermometer coding DAC is built of binary-to-thermometer decoder circuit. This DAC operate by converting the digital input code to thermometer code. The decoder will convert N-bit digital input into $2^N - 1$ number of bits in thermometer code. Only 1-bit

changes for each state-transition thus reducing the glitch problem. This DAC usually used in low resolution and not suitable in high resolution. This approach as mentioned in [11] have far better linearity, both Differential Non-Linearity (DNL) and Integral Non Linearity (INL), monotonicity and glitch performances.

The 12-bit hybrid DAC architecture utilized in this project composed of binary-weighted resistor DAC and thermometer coding DAC. The binary-weighted resistor scheme is representing the eight Least Significant Bit (LSB) whereas the thermometer coding scheme is used to represent four Most Significant Bit (MSB). Another architecture implemented in this hybrid DAC is the current steering scheme which composed of a switchable current source controlled by the digital input. All the current source is connected in parallel. This switchable current sources will provide sufficient current to the resistor network. This results in a 12-bit pseudo-differential hybrid DAC architecture which achieved improvement in linearity, better DNL and INL at the same time reducing glitches and overall area and circuit complexity. This Hybrid DAC has 12-bit resolution with DNL, 0.25 LSB and INL, 0.375 LSB, respectively [1].

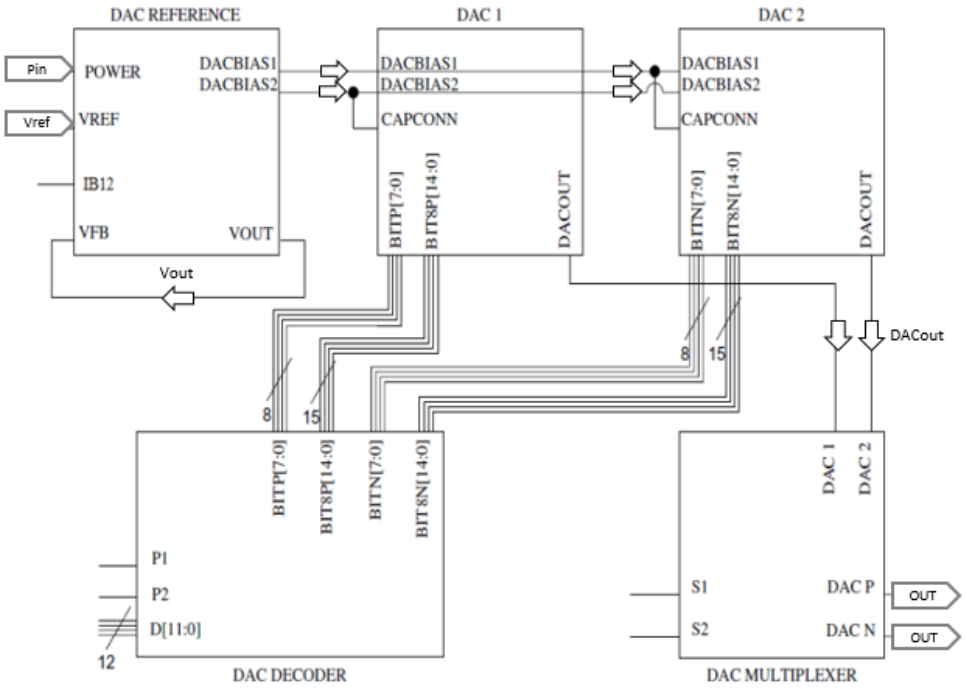


Figure 2.7:12-Bit Pseudo-Differential Hybrid DAC Architecture

Figure 2.1 presents the general block diagram of the hybrid DAC, and the interconnection between each block. There are five block in this hybrid DAC. The DAC Reference block is the most essential block providing constant bias voltage to the DAC 1 and DAC 2 . The Decoder is function to decode the 12-bit digital input from both DAC into an appropriate code, where 8-bit in LSB section and 15-bit of thermometer code in MSB [1]. The DAC blocks shown in Figure 2.1 are consisted of resistor string circuit and switchable current sources. As an important cell in the DAC block, the switchable current source composed of three PMOS transistors each with different width to length ratio (W/L) [1]. It responsible to provide constant current to the resistor string circuit when switched on.

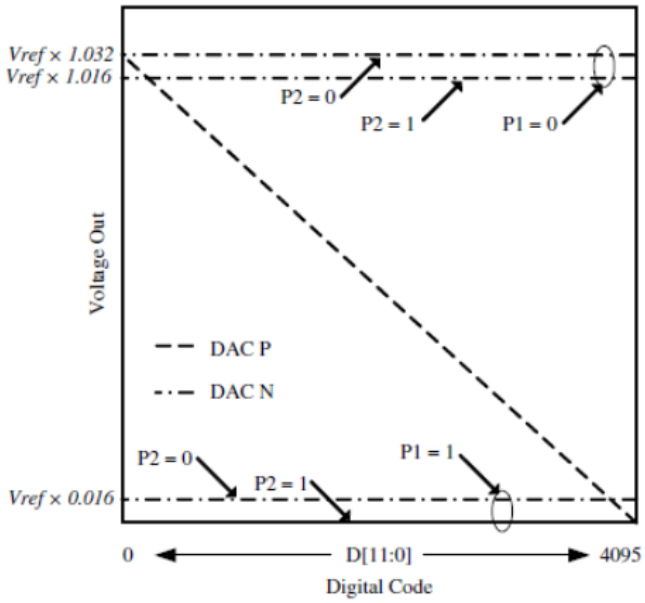


Figure 2. 8: Single DAC Transfer Characteristic [1]

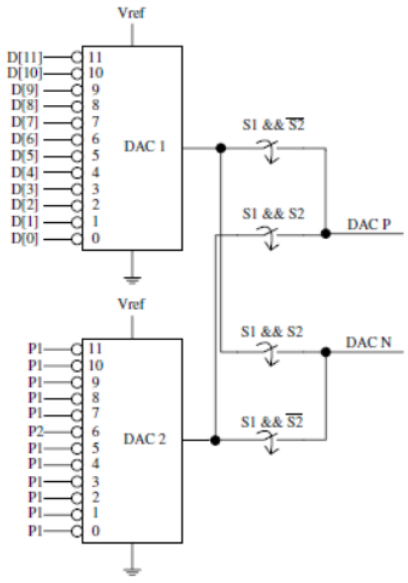


Figure 2.9: Pseudo-Differential DAC Block Diagram [1]

The pseudo-differential DAC block is consisted of two Single DAC blocks as present in Figure 2.3. The 12-bit digital input D[11:0] will controlled DAC 1 which divided into 8 LSB and 4 MSB segments. The DAC 2 however is controlled by both P1 and P2 which programmable to generate desired reference voltage [1]. The 8 bit digital input from LSB segment in DAC 1 is initially inverted from its original stage then supplied directly the binary weighted resistor string where resistance value increases for each bit [1].

Meanwhile the MSB segment of the DAC 1, a thermometer coding DAC is implemented at the top of the binary-weighted resistor string converting the 4-MSB input into 15-bit input in thermometer coding [1]. Every one of the 15-bit thermometer coding input is directly connected to two switchable current source. It will controlled the current flow from MSB section to the binary-weighted resistor string and the sum of these current flow will generate an output voltage level of the DAC block. Thus, as the 12 bit increases from 0 to 4095, DAC 1 output exponentially decrease from maximum of 737.1mV to zero volts as shown in Figure 2.2 [1]. The reference voltage Vref for this project is fixed at 737.1mV. The DAC 2 provide a constant reference voltage at Vref × 1.032, Vref × 1.016, Vref × 0.016 and 0 V as presented in Figure 2.2 which are controlled by programmable inputs P1 and P2 [2]. Finally, the output of the DACs are sourced to the DAC multiplexer and multiplexed according to the mode of operation set by input S1 and S2.

2.2.1 Switchable Current Source

The switchable current source is built of three PMOS transistors shown in Figure 2.4. PMOS transistor offers a lower 1/f-noise but a higher thermal noise level as results of the lower mobility of holes compared to electron [12]. It is best to have a current source with infinite output impedance. A cascoded-current cell has the capability to increase the output impedance. As shown in Figure 2.4 the transistors M1 and M2 are connected in cascaded structure in order to achieve high output impedance [5]. The constant bias voltages DACBIAS1 and DACBIAS2 are given by DAC Reference where each are 363.124 mV and 370.337mV, respectively [5]. The first bias voltage DACBIAS1 is functioned to control the source-gate voltage (V_{SG}) of transistor M1 setting nominal current through the switchable current source [5]. The second bias voltage DACBIAS2 is operating as a cascoded bias feeding in order to rise the output impedance of the current source.

The transistor M3 controlled by the input voltage level BITSEL at its gate terminal, when BITSEL is active '1' at high voltage, transistor M3 switched OFF but switchable current source is switched ON. Basically, transistor M3 is function as a switch to control mode operation of switchable current source. However when BITSEL is low '0' at low voltage level, transistor M3 is switched ON and switchable current source will be switched OFF. When transistor M3 is active it draws a constant current from transistor M1 to the

ground instead to output IOUT [5]. Meanwhile, the fourth terminal of resistor is connected to the supply voltage, Vdd which is fixed at 1.1V.

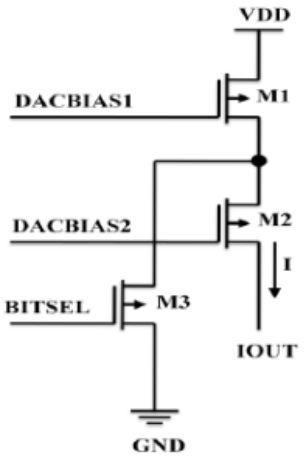


Figure 2.10: Switchable Current Source [5]

2.2.2 Binary-Weighted Resistor String

The binary-weighted resistor string is implemented in the 8-bit LSB segment of the hybrid DAC. Each value of the resistor is proportional to the weighted digital input bit value. As mentioned before the DAC output decreases from its full scale 737.1mV to 0V when digital input value incrementing from 0 to 4095 [5]. A 3-bit LSB structure is presented in Figure 2.5. As the input is at low logic level or '0', the switchable current source is switched ON generating a constant current with magnitude, *I* flowing through the resistor string [5]. As the value of resistors incrementing exponentially as the digital input bit increases, the outputs can be calculated using the superposition theorem [5].

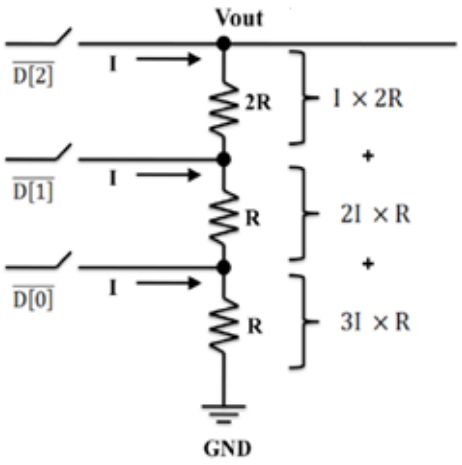


Figure 2.11: Simplified 3-bit structure of LSB segment [5]

From Figure 2.5, the simplified 3-bit LSB structure can be represented mathematically as shown in Equation (2.1). *I* referred as the magnitude of a constant current source, *R* is the LSB resistor and *D* is the digital input bit, which is '0' for low logic level and '1' for high logic level. This 3-bit structure can be extended to D[7] by incrementing the resistors value exponentially with corresponding digital input bits as shown in Figure 2.5 [5]. The 8-bit LSB structure can be represented mathematically as presented by Equation 2.1 and Equation 2.2.

$$V_{out} = (2^2 \overline{D[2]} + 2^1 \overline{D[1]} + 2^0 \overline{D[0]})(I \times R) \tag{2.1}$$

$$V_{out} = (2^7 \overline{D[7]} + 2^6 \overline{D[6]} + 2^5 \overline{D[5]} + 2^4 \overline{D[4]} + 2^3 \overline{D[3]} + 2^2 \overline{D[2]} + 2^1 \overline{D[1]} + 2^0 \overline{D[0]})(I \times R) \tag{2.2}$$

2.2.3 Thermometer Coding

The thermometer coding methodology is used in the 4-bit MSB segment of the hybrid DAC. In this thesis, the thermometer coding is implementing a 4-to-16 priority coding scheme. N-bit of digital input is converted to $2^N - 1$ number of bits in thermometer code. This results in the conversion of 4-bit MSB digital input into a 15-bit thermometer code is presented in Table 2.1.

In thermometer coding architecture, each of the bit in thermometer code is connected to two switchable current source, unlike the 8-bit LSB segment connected to only 1 current source for each bit [1]. Once the bit in thermometer code is active '1' or high logic level, the switchable current sources will be turned ON and the summation of the currents will flow to the weighted resistor string.

Table 2.2: Thermometer Coding for the 4-bit MSB segment [1]

D[11]	D[10]	D[9]	D[8]	THERMOMETER CODING
0	0	0	0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
0	0	0	1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0
0	0	1	0	1 1 1 1 1 1 1 1 1 1 1 1 1 0 0
0	0	1	1	1 1 1 1 1 1 1 1 1 1 1 1 0 0 0
0	1	0	0	1 1 1 1 1 1 1 1 1 1 1 0 0 0 0
0	1	0	1	1 1 1 1 1 1 1 1 1 1 0 0 0 0 0
0	1	1	0	1 1 1 1 1 1 1 1 1 0 0 0 0 0 0
0	1	1	1	1 1 1 1 1 1 1 1 0 0 0 0 0 0 0
1	0	0	0	1 1 1 1 1 1 1 0 0 0 0 0 0 0 0
1	0	0	1	1 1 1 1 1 1 0 0 0 0 0 0 0 0 0
1	0	1	0	1 1 1 1 1 0 0 0 0 0 0 0 0 0 0
1	0	1	1	1 1 1 1 0 0 0 0 0 0 0 0 0 0 0
1	1	0	0	1 1 1 0 0 0 0 0 0 0 0 0 0 0 0
1	1	0	1	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0
1	1	1	0	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1	1	1	1	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

For example, when the 4-bit MSB digital input *D*[11:8] is equal to 1110, it generated an equivalent thermometer code of 100000000000000. Each bit of the thermometer code is connected directly to two switchable current sources [1]. The high bit '1' will turns ON the switchable current sources. The equivalent total resistance of the weighted resistor string used in the 8-bit LSB segment as shown by Equation 2.3 and the output of DAC is equal to the result of Equation (2.4) [1].

$$R_{eq} = R + R + 2R + 4R + 8R + 16R + 32R + 64R = 128R \tag{2.3}$$

$$Vout = (2 \times 1)I \times Req = 2I \times 128R \tag{2.4}$$

As can be seen in the Equation (2.4), '1' in the bracket is actually represented the number of high bit in the thermometer coding. Therefore, it is multiplied by 2 as each high bit from the thermometer coding are connected to two switchable current source. The 4-MSB mathematical model represented in Equation (2.5). It can also be simplifies as in Equation (2.6) [1].

$$\begin{aligned} V_{\text{out}} = {} & (\overline{D[11]}(16I \times 128R) + \overline{D[10]}(8I \times 128R) + \overline{D[9]}(4I \times 128R) \\ & + \overline{D[8]}(2I \times 128R)) \end{aligned} \tag{2.5}$$

$$V_{\text{out}} = (2^{11}\overline{D[11]} + 2^{10}\overline{D[10]} + 2^{9}\overline{D[9]} + 2^{8}\overline{D[8]})(I \times R) \tag{2.6}$$

2.2.4 Hybrid DAC

The 12-bit hybrid DAC topology is consisted mainly of 8-LSB binary-weighted resistor DAC and 4-MSB thermometer coding DAC. This can be proven using the superposition theorem, the equivalent mathematical model of the 12 bit hybrid DAC can be represented by Equation (2.7), which obtained by simply adding both Equation (2.2) and Equation (2.6) [1]. The segmentation of the 12-bit hybrid DAC is presented in Figure 2.6. From the diagram it can be seen that the 8-bit LSB is placed at the bottom of the diagram while the 4-bit MSB is placed at top of the segment as can be seen in Figure 2.6.

$$V_{out} = \Big(2^{11}\,\overline{D[11]} + 2^{10}\,\overline{D[10]} + 2^{9}\,\overline{D[9]} + 2^{8}\,\overline{D[8]} + 2^{7}\,\overline{D[7]} + 2^{6}\,\overline{D[6]} + 2^{5}\,\overline{D[5]} + 2^{4}\,\overline{D[4]} + 2^{3}\,\overline{D[3]} + 2^{2}\,\overline{D[2]} + 2^{1}\,\overline{D[1]} + 2^{0}\,\overline{D[0]} \Big) (I \times R) \quad (2.7)$$

The target full scale output voltage for this 12 bit hybrid DAC is fixed to approximately 750mV. To calculate the magnitude of constant current source *I*, each bit of the 12-Bit D[11:0] digital input is fixed at a low logic level resulting a constant current *I* needed is 12.21 µA [1]. Therefore the magnitude of the constant current source for this project is fixed at 12 µA. Once it was fixed to a constant 12 µA with all digital inputs at low logic level. The full scale output voltage obtained from Equation (2.7) is 737.1mV and resolution of the 12 bit hybrid DAC is calculated to be 0.18 mV [1].

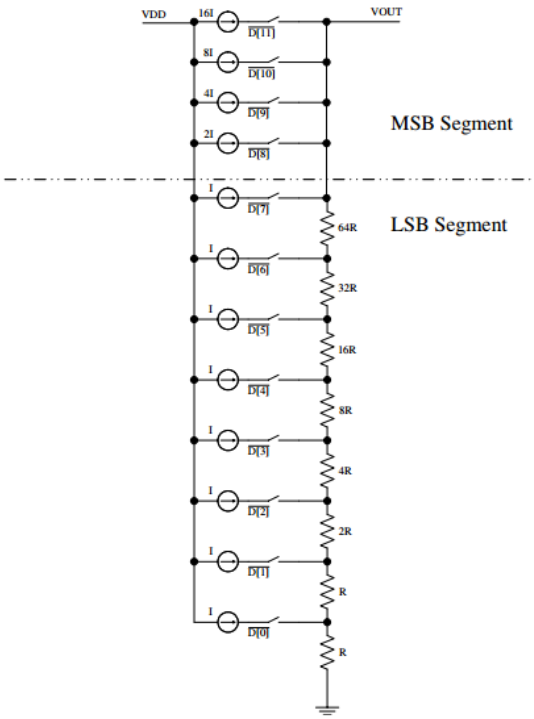


Figure 2.12: MSB and LSB segments of the 12-bit hybrid DAC [1]

2.3 Low Pass RC Filter

Glitches decreases the overall performance of a DAC. One known source glitches is the clock feed-through effect (CFT) effect which occur when switching control signal coupled with switch output terminal through parasitic capacitance [1]. This was reduced by introducing current-limited SRD which minimizes voltage swing of switching control signal that applied to switches [4]. However, it did not remove all glitches from the DAC as there are other factor contributing to the glitch phenomenon. Nevertheless, this project still implementing this current-limited SRD to minimize the

CFT effect. Maximum glitch impact tend to occur during major carry transition. As mentioned in Chapter 1, major carry transition is the point where single code transition resulting major changes in most significant bit (MSB) due to least significant bits (LSB).

Therefore a Low Pass Filter was introduced to further reduce the glitch phenomenon at the output. A Low Pass RC Filter is an analog filter function to smoothen an analog signal, therefore it is suitable to be implemented at the output of the DAC [13]. A resistor-capacitor network is basically a simple electric circuit that consist of capacitor and resistor driven by a current source. They function to filter out the unwanted signals. DAC output glitch referred to as "energy" are defined by both width and height of the pulse [14]. Knowing the width or pulse of the glitch is good enough to manipulate the shape of the glitch. Adding a simple RC filter as shown in Figure 2.7 at the DAC output will attenuated the amplitude of the glitch, causing the glitch to be smeared of smoothed [14].

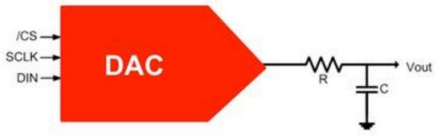
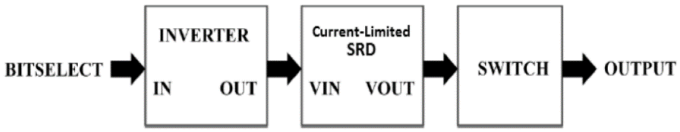
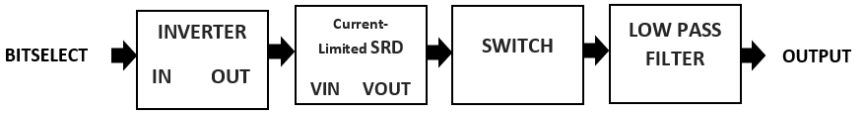


Figure 2.7: RC filter at DAC output [15]

a) Original DAC configuration [1]



b) Glitch improved DAC with Current-Limited SRD [1]



c) Glitch improved version DAC with Low Pass Filter

Figure 2.8: Block diagram of the proposed method

Figure 2.8 shows that the Low Pass Filter is placed at the switch output where it will filter out all the high frequency signal at the DAC output. The current-limited SRD is still remained between the decoder block and switchable current switches in order to minimize CFT effect [1]. The Low Pass Filter consists of two passive component of capacitor and resistor which allow low frequency signals to passes to the output while blocking the high frequency signals [15].

The resistor is positioned to be in series with the power sources while the capacitor to be in a parallel position with the same power source as shown in Figure 2.9. A capacitor is a reactive device meaning that the resistance it offer is depending to the frequency of the signal [15]. As the frequency applied to the capacitor increases, its reactance or